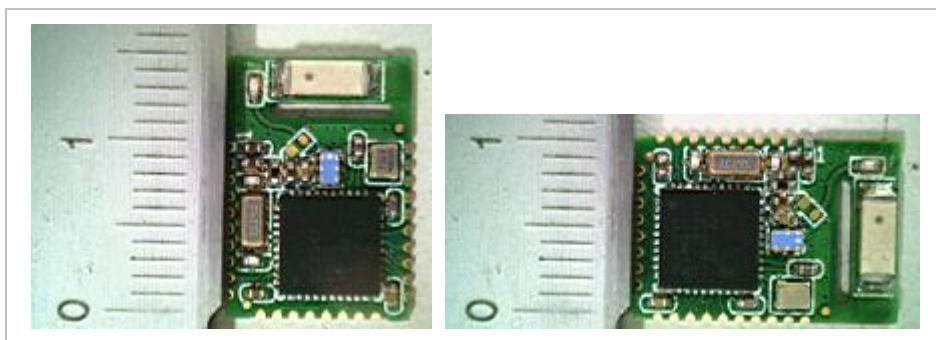


Bluetooth Low Energy Module Hardware Datasheet BLE0402C2P Rev 1.0



Chongqing JINOU Science and Technology Development Co., Ltd.

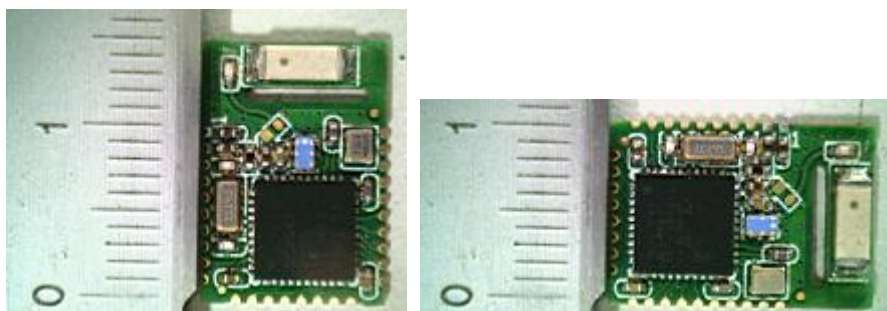
2015-03-10

Contents

1.	Features	2
2.	Product Description.....	2
3.	Applications	3
4.	Block Diagram	3
5.	Pin Descriptions	4
5.1	Device Terminal	4
5.2	Device Terminal Functions	4
6.	Electrical Specifications.....	5
6.1	ABSOLUTE MAXIMUM RATINGS	5
6.2	RECOMMENDED OPERATING CONDITIONS	5
6.3	ELECTRICAL CHARACTERISTICS	6
6.4	GENERAL CHARACTERISTICS	6
6.6	RF RECEIVE SECTION	7
6.7	RF TRANSMIT SECTION.....	9
6.8	ANALOG TEMPERATURE SENSOR	9
6.9	ADC CHARACTERISTICS	10
6.10	DC CHARACTERISTICS.....	11
7.	BLOCK DESCRIPTION	11
8.	Solder Profiles.....	14
9.	Physical Dimensions	15

Document History

Revision	Date	Change Reason
1.0	2015-03-10	create this document.
1.1	2015-04-24	Change to cc2541



1.Features

- True Single-Chip BLE Solution: CC2541 Can Run Both Application and BLE Protocol Stack, Includes Peripherals to Interface With Wide Range of Sensors ,Etc.
- Programmable Output Power Up to 4.5 dBm
- IR Generation Circuitry
- Powerful Five-Channel DMA
- 12-Bit ADC With Eight Channels and Configurable Resolution
- Two Powerful USARTs With Support for Several Serial Protocols
- 19 General-Purpose I/O Pins
- Low Power Mode:
 - Active Mode RX Down to 17.9mA
 - Active Mode TX (0 dBm): 18.2mA
 - Power Mode 1 (3-ms Wake-Up): 270 μ s
 - Power Mode 2 (Sleep Timer On): 1 μ s
 - Power Mode 3 (External Interrupts): 0.5 μ s
 - Wide Supply-Voltage Range (2V - 3.6V)

Full RAM and Register Retention in All Power Modes

- Nominal Supply Voltage at 3.3 \pm 0.1V
- Surface-mount, Size: 15.9 \times 11.2 (unit: mm error = \pm 0.2mm)

2.Product Description

The CC2541 is a power-optimized true system-on-chip (SoC) solution for both Bluetooth low energy and proprietary 2.4-GHz applications. It enables robust network nodes to be built with low total bill-of-material costs. The CC2541 combines the excellent performance of a leading RF transceiver with an industry-standard enhanced 8051 MCU, in-system programmable flash memory, 8-KB RAM, and many other powerful supporting features and peripherals.

The CC2541 is highly suited for systems where ultralow power consumption is required. This is

specified by various operating modes. Short transition times between operating modes further enable low power consumption.

Compared to the CC2540, the CC2541 provides lower RF current consumption. The CC2541 does not have the USB interface of the CC2540, and provides lower maximum output power in TX mode. The CC2541 also adds a HW I2C interface.

The CC2541 is pin-compatible with the CC2533 RF4CE-optimized IEEE 802.15.4 SoC.

The CC2541 comes in two different versions: CC2541F128/F256, with 128 KB and 256 KB of flash memory, respectively.

3.Applications

2.4-GHz *Bluetooth* low energy Systems

Mobile Phone Accessories

Sports and Leisure Equipment

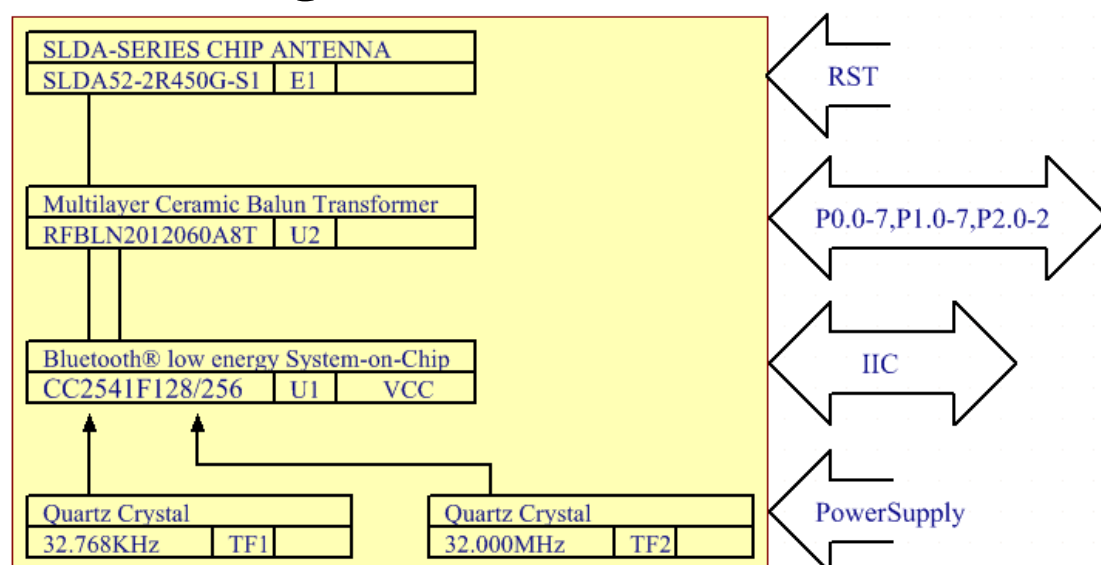
Consumer Electronics

Human Interface Devices(Keyboard,Mouse,Remote Control)

USB Dongles

Health Care and Medical

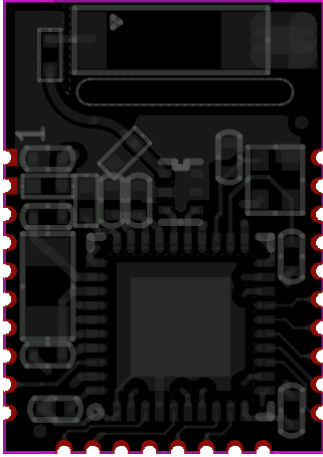
4.Block Diagram



Block Diagram

5.Pin Descriptions

5.1 Device Terminal

No.	Des					Des	No.
1	GND					RST	28
2	VCC					P0.0	27
3	NC					NC	26
4	NC					NC	25
5	P2.2					P0.1	24
6	P2.1					P0.2	23
7	P2.0					P0.3	22
8	P1.7					P0.4	21
9	P1.6					P0.5	20
10	SCL					P0.6	19
11	12	13	14	15	16	17	18
SDA	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	P0.7

5.2 Device Terminal Functions

PIN	NAME	PIN TYPE	DESCRIPTION
7	P2.0	Digital I/O	Port 2.0
6	P2.1 DD	Digital I/O	Port 2.1
		Debug Data	Debug data interface
5	P2.2 DC	Digital I/O	Port 2.2
		Debug Clock	Debug data interface
8	P1.7	Digital I/O	Port 1.7
9	P1.6	Digital I/O	Port 1.6
12	P1.5	Digital I/O	Port 1.5
13	P1.4	Digital I/O	Port 1.4
14	P1.3	Digital I/O	Port 1.3
15	P1.2	Digital I/O	Port 1.2
16	P1.1	Digital I/O	Port 1.1 20-mA drive capability
17	P1.0	Digital I/O	Port 1.0 20-mA drive capability
18	P0.7	Digital I/O	Port 0.7
19	P0.6	Digital I/O	Port 0.6
20	P0.5 RT	Digital O	UART request to send active low
		Digital I/O	Port 0.5
21	P0.4 CT	Digital I	UART clear to send active low
		Digital I/O	Port 0.4
22	P0.3 TX	Digital O	UART data output
		Digital I/O	Port 0.3
23	P0.2 RX	Digital I	UART data input

		Digital I/O	Port 0.2
24	P0.1	Digital I/O	Port 0.1
27	P0.0 A0	Analog I	ADC
		Digital I/O	Port 0.0
2	VCC	Power Supply	+3.3V Power Supply
1	GND	Ground	Connect to GND
28	RST	Digital input	Reset, active-low

6. Electrical Specifications

6.1 ABSOLUTE MAXIMUM RATINGS

		MIN	MAX	UNIT
Supply voltage	All supply pins must have the same voltage	−0.3	3.9	V
Voltage on any digital pin		−0.3	$V_{DD} + 0.3$, ≤ 3.9	V
Input RF level			10	dBm
Storage temperature range		−40	125	°C
ESD ₍₂₎	All pads, according to human-body model, JEDEC STD 22, method A114		2	kV
	According to charged-device model, JEDEC STD 22, method C101		500	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device.

These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) CAUTION: ESD-sensitive device. Precautions should be used when handling the device in order to prevent permanent damage.

6.2 RECOMMENDED OPERATING CONDITIONS

	MIN	MAX	UNIT
Operating ambient temperature range, T _A	−40	125	°C
Operating supply voltage	2	3.6	V

6.3 ELECTRICAL CHARACTERISTICS

Measured on Texas Instruments CC2541 EM reference design with $T_A = 25^\circ\text{C}$ and $V_{DD} = 3\text{ V}$,
1 Mbps, GFSK, 250-kHz deviation, Bluetooth low energy mode, and 0.1% BER

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{core} Core current consumption	RX mode, standard mode, no peripherals active, low MCU activity		17.9		mA
	RX mode, high-gain mode, no peripherals active, low MCU activity		20.2		
	TX mode, -20 dBm output power, no peripherals active, low MCU activity		16.8		
	TX mode, 0 dBm output power, no peripherals active, low MCU activity		18.2		
	Power mode 1. Digital regulator on; 16-MHz RCOSC and 32-MHz crystal oscillator off; 32.768-kHz XOSC, POR, BOD and sleep timer active; RAM and register retention		270		μA
	Power mode 2. Digital regulator off; 16-MHz RCOSC and 32-MHz crystal oscillator off; 32.768-kHz XOSC, POR, and sleep timer active; RAM and register retention		1		
	Power mode 3. Digital regulator off; no clocks; POR active; RAM and register retention		0.5		
	Low MCU activity: 32-MHz XOSC running. No radio or peripherals. Limited flash access, no RAM access.		6.7		mA
I_{peri} Peripheral current consumption (Adds to core current I_{core} for each peripheral unit activated)	Timer 1. Timer running, 32-MHz XOSC used		90		μA
	Timer 2. Timer running, 32-MHz XOSC used		90		
	Timer 3. Timer running, 32-MHz XOSC used		60		
	Timer 4. Timer running, 32-MHz XOSC used		70		
	Sleep timer, including 32.753-kHz RCOSC		0.6		
	ADC, when converting		1.2		mA

6.4 GENERAL CHARACTERISTICS

Measured on Texas Instruments CC2541 EM reference design with $T_A = 25^\circ\text{C}$ and $V_{DD} = 3\text{ V}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
WAKE-UP AND TIMING					
Power mode 1 → Active	Digital regulator on, 16-MHz RCOSC and 32-MHz crystal oscillator off. Start-up of 16-MHz RCOSC		4		μs
Power mode 2 or 3 → Active	Digital regulator off, 16-MHz RCOSC and 32-MHz crystal oscillator off. Start-up of regulator and 16-MHz RCOSC		120		μs
Active → TX or RX	Crystal ESR = 16 Ω. Initially running on 16-MHz RCOSC, with 32-MHz XOSC OFF		500		μs
	With 32-MHz XOSC initially on		180		μs
RX/TX turnaround	Proprietary auto mode		130		μs
	BLE mode		150		
RADIO PART					
RF frequency range	Programmable in 1-MHz steps	2379		2496	MHz
Data rate and modulation format	2 Mbps, GFSK, 500-kHz deviation 2 Mbps, GFSK, 320-kHz deviation 1 Mbps, GFSK, 250-kHz deviation 1 Mbps, GFSK, 160-kHz deviation 500 kbps, MSK 250 kbps, GFSK, 160-kHz deviation 250 kbps, MSK				

6.6 RF RECEIVE SECTION

Measured on Texas Instruments CC2541 EM reference design with $T_A = 25^\circ\text{C}$, $V_{DD} = 3\text{ V}$, $f_c = 2440\text{ MHz}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
2 Mbps, GFSK, 500-kHz Deviation, 0.1% BER					
Receiver sensitivity			-90		dBm
Saturation	BER < 0.1%		-1		dBm
Co-channel rejection	Wanted signal at -67 dBm		-9		dB
In-band blocking rejection	$\pm 2\text{ MHz}$ offset, 0.1% BER, wanted signal -67 dBm		-2		dB
	$\pm 4\text{ MHz}$ offset, 0.1% BER, wanted signal -67 dBm		36		
	$\pm 6\text{ MHz}$ or greater offset, 0.1% BER, wanted signal -67 dBm		41		
Frequency error tolerance ⁽¹⁾	Including both initial tolerance and drift. Sensitivity better than -67dBm, 250 byte payload. BER 0.1%	-300		300	kHz
Symbol rate error tolerance ⁽²⁾	Maximum packet length. Sensitivity better than -67dBm, 250 byte payload. BER 0.1%	-120		120	ppm
2 Mbps, GFSK, 320-kHz Deviation, 0.1% BER					
Receiver sensitivity			-86		dBm
Saturation	BER < 0.1%		-7		dBm
Co-channel rejection	Wanted signal at -67 dBm		-12		dB
In-band blocking rejection	$\pm 2\text{ MHz}$ offset, 0.1% BER, wanted signal -67 dBm		-1		dB
	$\pm 4\text{ MHz}$ offset, 0.1% BER, wanted signal -67 dBm		34		
	$\pm 6\text{ MHz}$ or greater offset, 0.1% BER, wanted signal -67 dBm		39		
Frequency error tolerance ⁽¹⁾	Including both initial tolerance and drift. Sensitivity better than -67 dBm, 250 byte payload. BER 0.1%	-300		300	kHz
Symbol rate error tolerance ⁽²⁾	Maximum packet length. Sensitivity better than -67 dBm, 250 byte payload. BER 0.1%	-120		120	ppm

(1) Difference between center frequency of the received RF signal and local oscillator frequency

(2) Difference between incoming symbol rate and the internally generated symbol rate

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
1 Mbps, GFSK, 250-kHz Deviation, Bluetooth low energy Mode, 0.1% BER					
Receiver sensitivity ⁽³⁾⁽⁴⁾	High-gain mode		-94		dBm
	Standard mode		-88		
Saturation ⁽⁴⁾	BER < 0.1%		5		dBm
Co-channel rejection ⁽⁴⁾	Wanted signal -67 dBm		-6		dB
In-band blocking rejection ⁽⁴⁾	±1 MHz offset, 0.1% BER, wanted signal -67 dBm		-2		dB
	±2 MHz offset, 0.1% BER, wanted signal -67 dBm		26		
	±3 MHz offset, 0.1% BER, wanted signal -67 dBm		34		
	>6 MHz offset, 0.1% BER, wanted signal -67 dBm		33		
Out-of-band blocking rejection ⁽⁴⁾	Minimum interferer level < 2 GHz (Wanted signal -67 dBm)		-21		dBm
	Minimum interferer level [2 GHz, 3 GHz] (Wanted signal -67 dBm)		-25		
	Minimum interferer level > 3 GHz (Wanted signal -67 dBm)		-7		
Intermodulation ⁽⁴⁾	Minimum interferer level		-36		dBm
Frequency error tolerance ⁽⁵⁾	Including both initial tolerance and drift. Sensitivity better than -67dBm, 250 byte payload. BER 0.1%	-250		250	kHz
Symbol rate error tolerance ⁽⁶⁾	Maximum packet length. Sensitivity better than -67 dBm, 250 byte payload. BER 0.1%	-80		80	ppm
1 Mbps, GFSK, 160-kHz Deviation, 0.1% BER					
Receiver sensitivity ⁽⁷⁾			-91		dBm
Saturation	BER < 0.1%		0		dBm
Co-channel rejection	Wanted signal 10 dB above sensitivity level		-9		dB
In-band blocking rejection	±1-MHz offset, 0.1% BER, wanted signal -67 dBm		2		dB
	±2-MHz offset, 0.1% BER, wanted signal -67 dBm		24		
	±3-MHz offset, 0.1% BER, wanted signal -67 dBm		27		
	>6-MHz offset, 0.1% BER, wanted signal -67 dBm		32		
Frequency error tolerance ⁽⁵⁾	Including both initial tolerance and drift. Sensitivity better than -67 dBm, 250-byte payload. BER 0.1%	-200		200	kHz
Symbol rate error tolerance ⁽⁶⁾	Maximum packet length. Sensitivity better than -67 dBm, 250-byte payload. BER 0.1%	-80		80	ppm
500 kbps, MSK, 0.1% BER					
Receiver sensitivity ⁽⁷⁾			-99		dBm
Saturation	BER < 0.1%		0		dBm
Co-channel rejection	Wanted signal -67 dBm		-5		dB
In-band blocking rejection	±1-MHz offset, 0.1% BER, wanted signal -67 dBm		20		dB
	±2-MHz offset, 0.1% BER, wanted signal -67 dBm		27		
	>2-MHz offset, 0.1% BER, wanted signal -67 dBm		28		
Frequency error tolerance	Including both initial tolerance and drift. Sensitivity better than -67 dBm, 250-byte payload. BER 0.1%	-150		150	kHz
Symbol rate error tolerance	Maximum packet length. Sensitivity better than -67 dBm, 250-byte payload. BER 0.1%	-80		80	ppm

(3) The receiver sensitivity setting is programmable using a TI BLE stack vendor-specific API command. The default value is standard mode.

(4) Results based on standard-gain mode.

(5) Difference between center frequency of the received RF signal and local oscillator frequency

(6) Difference between incoming symbol rate and the internally generated symbol rate

(7) Results based on high-gain mode.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
250 kbps, GFSK, 160 kHz Deviation, 0.1% BER					
Receiver sensitivity ⁽⁸⁾			-98		dBm
Saturation	BER < 0.1%		0		dBm
Co-channel rejection	Wanted signal -67 dBm		-3		dB
In-band blocking rejection	±1-MHz offset, 0.1% BER, wanted signal -67 dBm		23		dB
	±2-MHz offset, 0.1% BER, wanted signal -67 dBm		28		
	>2-MHz offset, 0.1% BER, wanted signal -67 dBm		29		
Frequency error tolerance ⁽⁹⁾	Including both initial tolerance and drift. Sensitivity better than -67 dBm, 250-byte payload. BER 0.1%	-150		150	kHz
Symbol rate error tolerance ⁽¹⁰⁾	Maximum packet length. Sensitivity better than -67 dBm, 250-byte payload. BER 0.1%	-80		80	ppm
250 kbps, MSK, 0.1% BER					
Receiver sensitivity ⁽¹¹⁾			-99		dBm
Saturation	BER < 0.1%		0		dBm
Co-channel rejection	Wanted signal -67 dBm		-5		dB
In-band blocking rejection	±1-MHz offset, 0.1% BER, wanted signal -67 dBm		20		dB
	±2-MHz offset, 0.1% BER, wanted signal -67 dBm		29		
	>2-MHz offset, 0.1% BER, wanted signal -67 dBm		30		
Frequency error tolerance	Including both initial tolerance and drift. Sensitivity better than -67 dBm, 250-byte payload. BER 0.1%	-150		150	kHz
Symbol rate error tolerance	Maximum packet length. Sensitivity better than -67 dBm, 250-byte payload. BER 0.1%	-80		80	ppm
ALL RATES/FORMATS					
Spurious emission in RX. Conducted measurement	f < 1 GHz		-67		dBm
Spurious emission in RX. Conducted measurement	f > 1 GHz		-57		dBm

(8) Results based on standard-gain mode.

(9) Difference between center frequency of the received RF signal and local oscillator frequency

(10) Difference between incoming symbol rate and the internally generated symbol rate

(11) Results based on high-gain mode.

6.7 RF TRANSMIT SECTION

Measured on Texas Instruments CC2541 EM reference design with $T_A = 25^\circ\text{C}$, $V_{DD} = 3\text{ V}$ and $f_c = 2440\text{ MHz}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output power	Delivered to a single-ended 50-Ω load through a balun using maximum recommended output power setting		0		dBm
	Delivered to a single-ended 50-Ω load through a balun using minimum recommended output power setting		-20		
Programmable output power range	Delivered to a single-ended 50-Ω load through a balun using minimum recommended output power setting		20		dB
Spurious emission conducted measurement	f < 1 GHz		-52		dBm
	f > 1 GHz		-48		dBm
	Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan)				
Optimum load impedance	Differential impedance as seen from the RF port (RF_P and RF_N) toward the antenna		70 +j30		Ω

Designs with antenna connectors that require conducted ETSI compliance at 64 MHz should insert an LC resonator in front of the antenna connector. Use a 1.6-nH inductor in parallel with a 1.8-pF capacitor. Connect both from the signal trace to a good RF ground.

6.8 ANALOG TEMPERATURE SENSOR

Measured on Texas Instruments CC2541 EM reference design with $T_A = 25^\circ\text{C}$ and $V_{DD} = 3\text{ V}$

	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output at 25 °C			1480		12-bit ADC
Temperature coefficient			4.5		/1 °C
Voltage coefficient			1		/0.1 V
Initial accuracy without calibration	Measured using integrated ADC, using internal bandgap voltage reference and		±10		°C
Accuracy using 1-point calibration (entire temperature range)	maximum resolution		±5		°C
Current consumption when enabled (ADC current not included)			0.5		mA

6.9 ADC CHARACTERISTICS

TA = 25 °C and VDD = 3 V, All measurement results are obtained using the CC2541 reference designs, post-calibration.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Common-mode maximum voltage			VDD		V
Common-mode minimum voltage			−0.3		
Input offset voltage			1		mV
Offset vs temperature			16		μV/°C
Offset vs operating voltage			4		mV/V
Supply current			230		nA
Hysteresis			0.15		mV

TA = 25 °C and VDD = 3 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage	VDD is voltage on AVDD5 pin	0		VDD	V
External reference voltage	VDD is voltage on AVDD5 pin	0		VDD	V
External reference voltage differential	VDD is voltage on AVDD5 pin	0		VDD	V
Input resistance, signal	Simulated using 4-MHz clock speed		197		kΩ
Full-scale signal ⁽¹⁾	Peak-to-peak, defines 0 dBFS		2.97		V
ENOB ⁽¹⁾ Effective number of bits	Single-ended input, 7-bit setting		5.7		bits
	Single-ended input, 9-bit setting		7.5		
	Single-ended input, 10-bit setting		9.3		
	Single-ended input, 12-bit setting		10.3		
	Differential input, 7-bit setting		6.5		
	Differential input, 9-bit setting		8.3		
	Differential input, 10-bit setting		10		
	Differential input, 12-bit setting		11.5		
	10-bit setting, clocked by RCOSC		9.7		
	12-bit setting, clocked by RCOSC		10.9		
Useful power bandwidth	7-bit setting, both single and differential		0–20		kHz
THD Total harmonic distortion	Single ended input, 12-bit setting, −6 dBFS ⁽¹⁾		−75.2		dB
	Differential input, 12-bit setting, −6 dBFS ⁽¹⁾		−86.6		
Signal to nonharmonic ratio	Single-ended input, 12-bit setting ⁽¹⁾		70.2		dB
	Differential input, 12-bit setting ⁽¹⁾		79.3		
	Single-ended input, 12-bit setting, −6 dBFS ⁽¹⁾		78.8		
	Differential input, 12-bit setting, −6 dBFS ⁽¹⁾		88.9		

CMRR	Common-mode rejection ratio	Differential input, 12-bit setting, 1-kHz sine (0 dBFS), limited by ADC resolution	>84			dB	
	Crosstalk	Single ended input, 12-bit setting, 1-kHz sine (0 dBFS), limited by ADC resolution	>84			dB	
	Offset	Midscale	−3			mV	
	Gain error		0.68%				
DNL	Differential nonlinearity	12-bit setting, mean ⁽¹⁾	0.05			LSB	
		12-bit setting, maximum ⁽¹⁾	0.9				
INL	Integral nonlinearity	12-bit setting, mean ⁽¹⁾	4.6			LSB	
		12-bit setting, maximum ⁽¹⁾	13.3				
		12-bit setting, mean, clocked by RCOSC	10				
		12-bit setting, max, clocked by RCOSC	29				
SINAD (−THD+N)	Signal-to-noise-and-distortion	Single ended input, 7-bit setting ⁽¹⁾	35.4			dB	
		Single ended input, 9-bit setting ⁽¹⁾	46.8				
		Single ended input, 10-bit setting ⁽¹⁾	57.5				
		Single ended input, 12-bit setting ⁽¹⁾	66.6				
		Differential input, 7-bit setting ⁽¹⁾	40.7				
		Differential input, 9-bit setting ⁽¹⁾	51.6				
		Differential input, 10-bit setting ⁽¹⁾	61.8				
		Differential input, 12-bit setting ⁽¹⁾	70.8				
	Conversion time	7-bit setting	20			μs	
		9-bit setting	36				
		10-bit setting	68				
		12-bit setting	132				
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Power consumption					1.2		mA
Internal reference VDD coefficient					4		mV/V
Internal reference temperature coefficient					0.4		mV/10°C
Internal reference voltage					1.15		V

6.10 DC CHARACTERISTICS

TA = 25 °C, VDD = 3 V, unless otherwise noted.

	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Logic-0 input voltage				0.5	V
Logic-1 input voltage		2.4			V
Logic-0 input current	Input equals 0 V	−50		50	nA
Logic-1 input current	Input equals VDD	−50		50	nA
I/O-pin pullup and pulldown resistors			20		kΩ
Logic-0 output voltage, 4-mA pins	Output load 4 mA			0.5	V
Logic-1 output voltage, 4-mA pins	Output load 4 mA	2.5			V
Logic-0 output voltage, 20-mA pins	Output load 20 mA			0.5	V
Logic-1 output voltage, 20-mA pins	Output load 20 mA	2.5			V

7.BLOCK DESCRIPTION

CPU and Memory

The **8051 CPU core** is a single-cycle 8051-compatible core. It has three different memory access busses

(SFR, DATA, and CODE/XDATA), a debug interface, and an 18-input extended interrupt unit.

The **memory arbiter** is at the heart of the system, as it connects the CPU and DMA controller with the physical memories and all peripherals through the SFR bus. The memory arbiter has four memory-access points, access of which can map to one of three physical memories: an SRAM, flash memory, and XREG/SFR registers. It is responsible for performing arbitration and sequencing between simultaneous memory accesses to the same physical memory.

The **SFR bus** is drawn conceptually in Figure 8 as a common bus that connects all hardware peripherals to the memory arbiter. The SFR bus in the block diagram also provides access to the radio registers in the radio register bank, even though these are indeed mapped into XDATA memory space.

The **8-KB SRAM** maps to the DATA memory space and to parts of the XDATA memory spaces. The SRAM is an ultralow-power SRAM that retains its contents even when the digital part is powered off (power modes 2 and 3).

The **128/256 KB flash block** provides in-circuit programmable non-volatile program memory for the device, and maps into the CODE and XDATA memory spaces.

Peripherals

Writing to the flash block is performed through a **flash controller** that allows page-wise erasure and 4-bitwise programming. See User Guide for details on the flash controller.

A versatile five-channel **DMA controller** is available in the system, accesses memory using the XDATA memory space, and thus has access to all physical memories. Each channel (trigger, priority, transfer mode, addressing mode, source and destination pointers, and transfer count) is configured with DMA descriptors that can be located anywhere in memory. Many of the hardware peripherals (AES core, flash controller, USARTs, timers, ADC interface, etc.) can be used with the DMA controller for efficient operation by performing data transfers between a single SFR or XREG address and flash/SRAM.

Each CC2540/1 contains a unique 48-bit IEEE address that can be used as the public device address for a *Bluetooth* device. Designers are free to use this address, or provide their own, as described in the *Bluetooth* specification.

The **interrupt controller** services a total of 18 interrupt sources, divided into six interrupt groups, each of which is associated with one of four interrupt priorities. I/O and sleep timer interrupt requests are serviced even if the device is in a sleep mode (power modes 1 and 2) by bringing the CC2540/1 back to the active mode.

The **debug interface** implements a proprietary two-wire serial interface that is used for in-circuit debugging. Through this debug interface, it is possible to erase or program the entire flash memory, control which oscillators are enabled, stop and start execution of the user program, execute instructions on the 8051 core, set code breakpoints, and single-step through instructions in the code. Using these techniques, it is possible to perform in-circuit debugging and external flash programming elegantly.

The **I/O controller** is responsible for all general-purpose I/O pins. The CPU can configure whether peripheral modules control certain pins or whether they are under software control, and if so, whether each pin is configured as an input or output and if a pullup or pulldown resistor in the pad is connected. Each peripheral that connects to the I/O pins can choose between two different I/O pin locations to ensure flexibility in various applications.

The **sleep timer** is an ultralow-power timer that can either use an external 32.768-kHz crystal oscillator

or an internal 32.753-kHz RC oscillator. The sleep timer runs continuously in all operating modes except power mode

3. Typical applications of this timer are as a real-time counter or as a wake-up timer to get out of power modes 1 or 2.

A built-in **watchdog timer** allows the CC2540/1 to reset itself if the firmware hangs. When enabled by software, the watchdog timer must be cleared periodically; otherwise, it resets the device when it times out.

Timer 1 is a 16-bit timer with timer/counter/PWM functionality. It has a programmable prescaler, a 16-bit period value, and five individually programmable counter/capture channels, each with a 16-bit compare value. Each of the counter/capture channels can be used as a PWM output or to capture the timing of edges on input signals. It can also be configured in IR generation mode, where it counts timer 3 periods and the output is ANDed with the output of timer 3 to generate modulated consumer IR signals with minimal CPU interaction.

Timer 2 is a 40-bit timer used by the *Bluetooth* low energy stack. It has a 16-bit counter with a configurable timer period and a 24-bit overflow counter that can be used to keep track of the number of periods that have transpired. A 40-bit capture register is also used to record the exact time at which a start-of-frame delimiter is received/transmitted or the exact time at which transmission ends. There are two 16-bit timer-compare registers and two 24-bit overflow-compare registers that can be used to give exact timing for start of RX or TX to the radio or general interrupts.

Timer 3 and timer 4 are 8-bit timers with timer/counter/PWM functionality. They have a programmable prescaler, an 8-bit period value, and one programmable counter channel with an 8-bit compare value. Each of the counter channels can be used as PWM output.

USART 0 and USART 1 are each configurable as either an SPI master/slave or a UART. They provide double buffering on both RX and TX and hardware flow control and are thus well suited to high-throughput full-duplex applications. Each USART has its own high-precision baud-rate generator, thus leaving the ordinary timers free for other uses. When configured as SPI slaves, the USARTs sample the input signal using SCK directly instead of using some oversampling scheme, and are thus well-suited for high data rates.

The **AES encryption/decryption core** allows the user to encrypt and decrypt data using the AES algorithm with 128-bit keys. The AES core also supports ECB, CBC, CFB, OFB, CTR, and CBC-MAC, as well as hardware support for CCM.

The **ADC** supports 7 to 12 bits of resolution with a corresponding range of bandwidths from 30-kHz to 4-kHz, respectively. DC and audio conversions with up to eight input channels (I/O controller pins) are possible. The inputs can be selected as single-ended or differential. The reference voltage can be internal, AVDD, or a single-ended or differential external signal. The ADC also has a temperature-sensor input channel. The ADC can automate the process of periodic sampling or conversion over a sequence of channels.

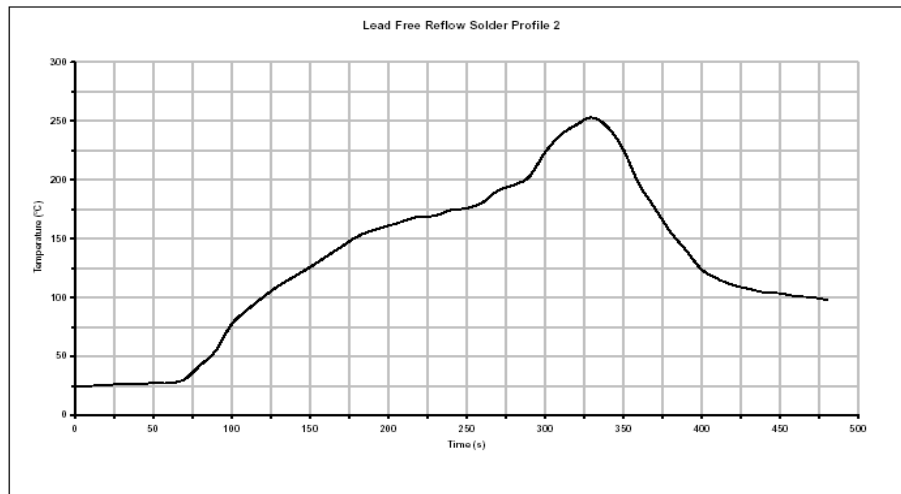
The **operational amplifier** is intended to provide front-end buffering and gain for the ADC. Both inputs as well as the output are available on pins, so the feedback network is fully customizable. A chopper-stabilized mode is available for applications that need good accuracy with high gain.

The ultralow-power **analog comparator** enables applications to wake up from PM2 or PM3 based on an analog signal. Both inputs are brought out to pins; the reference voltage must be provided

externally. The comparator output is connected to the I/O controller interrupt detector and can be treated by the MCU as a regular I/O pin interrupt

8. Solder Profiles

Composition of the solder ball: Sn 95.5%, Ag 4.0%, Cu 0.5%



Typical Lead-Free Re-flow Solder Profile

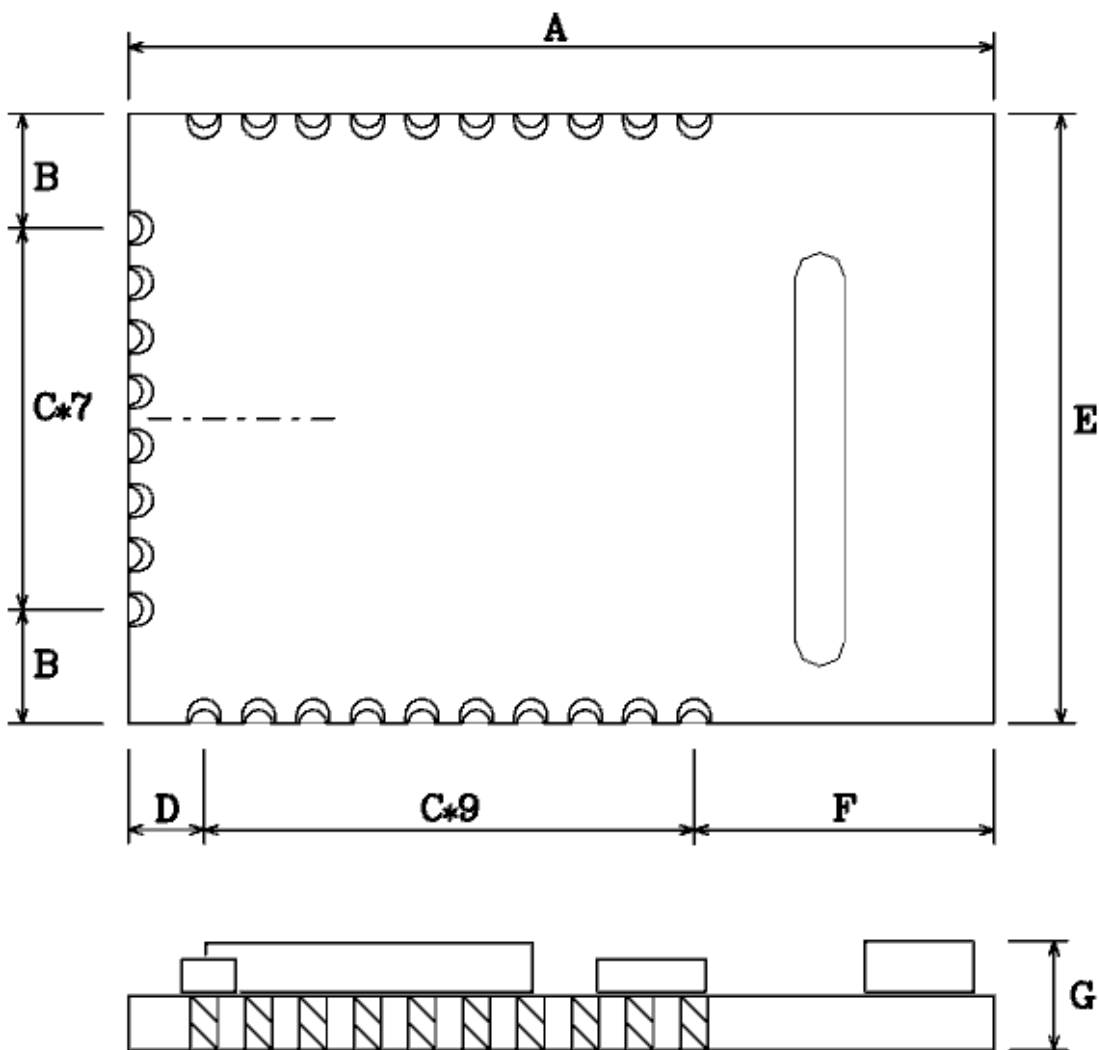
Key features of the profile:

- Initial Ramp = 1-2.5 °C/sec to 175 °C ± 25 °C equilibrium
- Equilibrium time = 60 to 180 seconds
- Ramp to Maximum temperature (250 °C) = 3 °C/sec max.
- Time above liquidus temperature (217 °C): 45-90 seconds
- Device absolute maximum reflow temperature: 260 °C

Devices will withstand the specified profile. Lead-free devices will withstand up to three reflows to a maximum temperature of 260 °C.

Notes: They need to be baked prior to mounting.

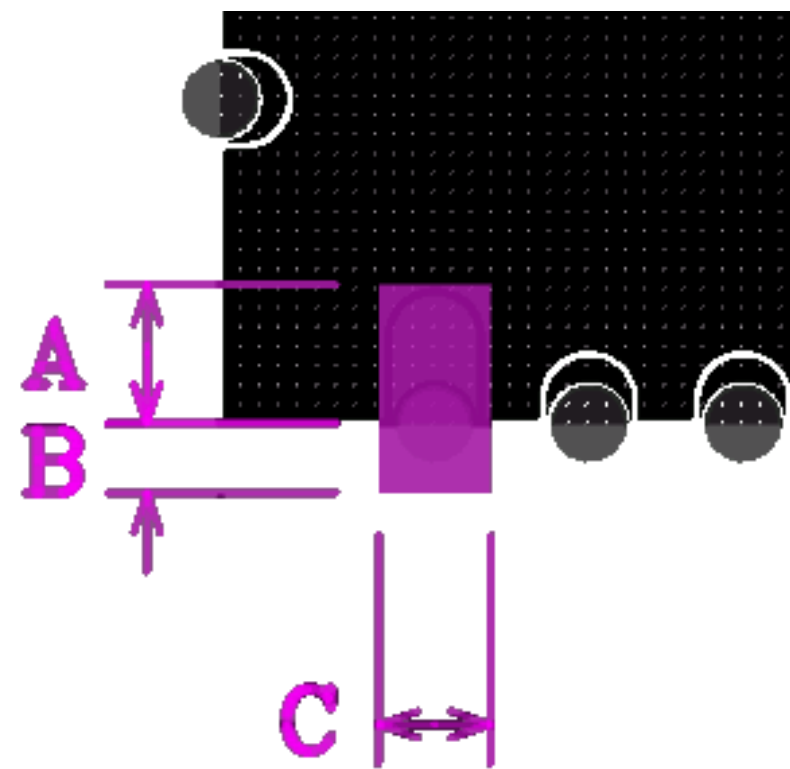
9. Physical Dimensions



A	B	C	D	E	F	G	
15.9	2.1	1.0	1.4	11.2	5.5	2.0	mm
625.98	82.68	39.37	55.12	440.94	216.54	78.74	mil

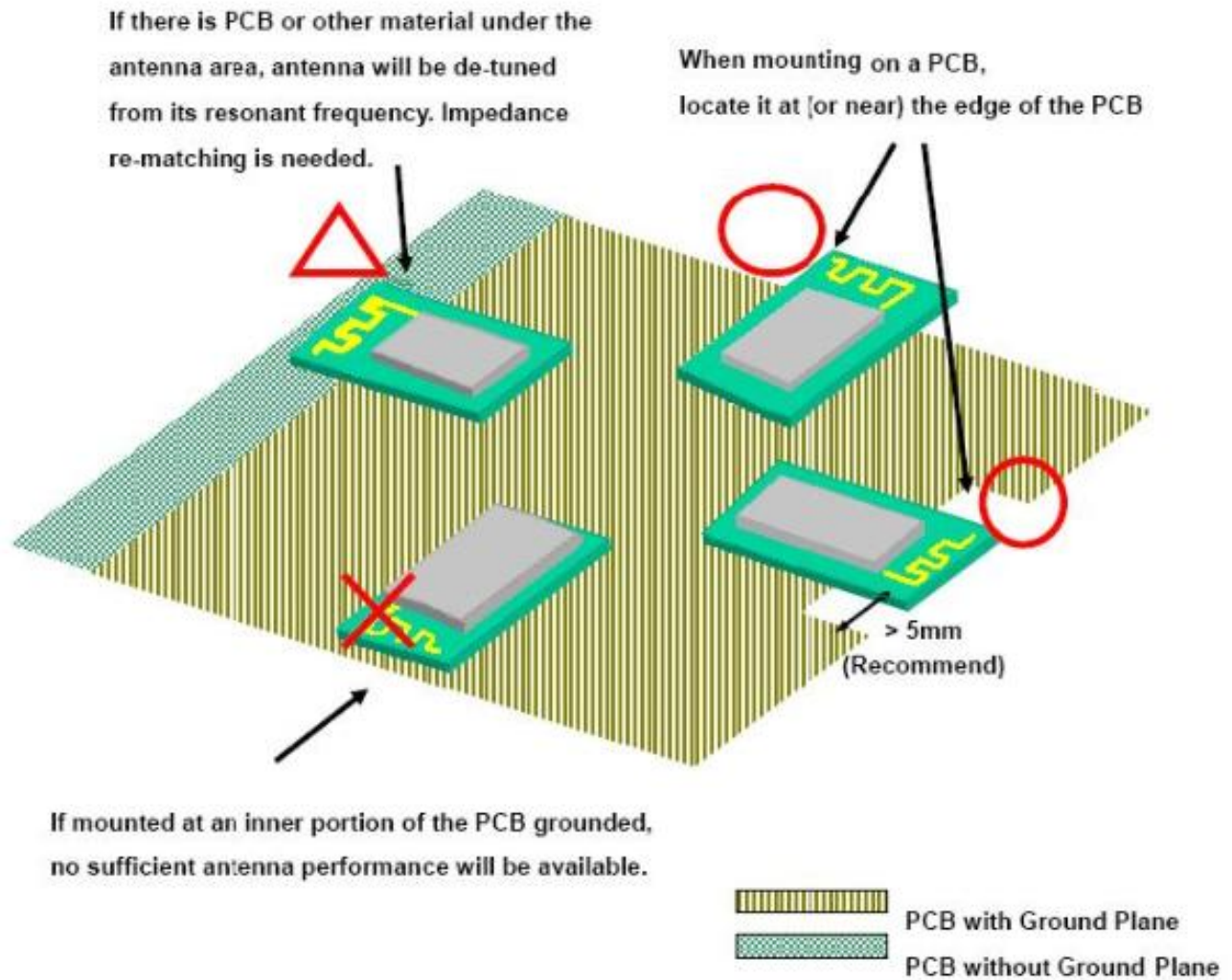
Deviation: $\pm 0.2\text{mm}$

Recommend PCB Layout



A	B	C	
0.90	0.45	0.72	mm
35.43	17.72	28.35	mil

Deviation: $\pm 0.1\text{mm}$



Chongqing Jinou Science & Technology Development Co., Ltd.

Add: 12-2-1-1, Huaxuan Branch Road 108#, Yuzhou Road, Jiulongpo District, Chongqing, 400041, China.

Tel: 86-23-68903066/68842136

Fax: 86-23-68644164

Web: www.jinoux.com www.oemblue.com